AF/2815

#14 Appeal Brief 10/8/03 AG

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:		Conf. No.:	3433
	Kazuaki Ano	Docket No.:	TI-33184
Serial No.:	09/930,361	Examiner:	Landau, M. C.
Filed:	08/15/2001	Art Unit:	2815

For: Low Profile Ball-Grid Array Package for High Power

Appeal Brief

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

MAILING CERTIFICATE UNDER 37 C.F.R. §1.8(A)
I hereby certify that this correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450 on
October 6, 2003.
Elizabeth Austin

Dear Sir:

Pursuant to the Notice of Appeal mailed 08/06/03, Appellant submits this appeal brief in triplicate. The Commissioner is hereby requested and authorized to charge any fees necessary for the filing of the enclosed papers to deposit account number 20-0668 of Texas Instruments Incorporated.

Real Party in Interest

The real party in interest is Texas Instruments Incorporated.

Related Appeals and Interferences

No related appeals or interferences are known to Appellant.

Status of Claims

Claims 1-11 and 18-26 are pending in this application. Claim 7 has been allowed and Claims 12-17 have been cancelled. Claims 1-6, 8-11, and 18-26 are the subject of this appeal.

Claim 19 stands rejected under 35 U.S.C. 112, second paragraph.

Claims 1, 2, 4-6, and 18 stand rejected under 35 U.S.C. 102(b) as being anticipated by Johnson (U.S. Patent No. 5,888,849).

Claim 3 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson in view of Ikegami (U.S. Patent No. 6,194,781).

Claims 8-11 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson in view of Cheng (U.S. Publ. Pat. Appl. 2002/0066592).

Claims 19-24 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson in view of Carter, Jr., et al. (U.S. Patent No. 5,594,234).

Claims 25 and 26 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson in view of Cheng and Carter.

Status of Amendments

All amendments have been entered.

Summary of Invention

One embodiment of the invention is a packaged integrated circuit chip (100 in Figure 1). The packaged chip includes a substrate 101 having first 101a and second 101b opposing surfaces with an opening 104 extending through the substrate from the first surface to the second surface. A chip mount pad of metal foil 105 is attached to the first surface of the substrate and is downset into

and covers the opening 104 such that a bottom surface of the chip mount pad is coplanar with the second surface 101b of the substrate. An integrated circuit chip 106 is mounted on a top surface of the chip mount pad. Encapsulation 108 is on the first surface 101a of the substrate and is not on the second surface 101b of the substrate, such that the encapsulation covers the chip, but does not cover the bottom surface of the chip mount pad. This arrangement retains the advantages of a plastic-substrate package while also allowing the direct connection of a heat sink to the exposed chip mount pad. The reader is particularly referred to the text of the specification corresponding to Figures 1 and 2, from line 9 of page 6 through line 20 of page 9 for further details.

Issues

1. Whether Claim 19 is patentable under 35 U.S.C. 112, second paragraph.

2. Whether Claims 1, 2, 4-6, and 18 are patentable under 35 U.S.C. 102(b) over Johnson.

3. Whether Claim 3 is patentable under 35 U.S.C. 103(a) over Johnson in view of Ikegami.

4. Whether Claims 8-11 are patentable under 35 U.S.C. 103(a) over Johnson in view of Cheng.

5. Whether Claims 19-24 are patentable under 35 U.S.C. 103(a) over Johnson in view of Carter.

6. Whether Claims 25 and 26 are patentable under 35 U.S.C. 103(a) over Johnson in view of Cheng and Carter.

Grouping of Claims

Claims 1-6 stand or fall together. Claims 8-11 and 18-21 stand or fall together. Claims 22-26 stand or fall together. Each of these groups of claims stand or fall independently of any other group of claims.

Argument

1. Claim 19 is patentable under 35 U.S.C. 112, second paragraph.

. The Examiner asserted that Claim 19 is unclear where it states that encapsulant that covers at least a portion of the first surface of the substrate does not cover the second surface of the substrate and does not cover "said portion of said sheet metal in said opening coplanar with said second surface of said substrate." Applicant respectfully points out that the claim refers to first and second surfaces of the substrate which correspond to the top and bottom surfaces, respectively, of substrate 101 shown in Figure 1. Encapsulant 108 covers the top surface of the substrate 101 and even a portion of the top surface of sheet metal 105b, but clearly does not cover the bottom surface of substrate 101 or the bottom surface of sheet metal 105b, which is coplanar with the bottom surface of substrate 101. Appellant submits that the claim language is therefore clear and supported by the specification, including Figure 1.

2. Claims 1, 2, 4-6, and 18 are patentable under 35 U.S.C. 102(b) over Johnson.

Claim 1 is to a "reel-to-reel tape." Johnson includes the statement "[t]he stiffener makes it possible to handle the flexible film in strips, rolls or small panels" (col. 3, line 5), but does not disclose a reel-to-reel tape. Claim 1 includes the feature of "a chip mount pad, secured to said first surface, coplanar with said second surface." Johnson does not disclose such a chip mount pad. Note that element 10 in Johnson's Figure 6 is a lead, not a mount pad. The

clear lack of physical support for chip 6 other than by leads 10 is a likely reason for Johnson's use of encapsulant 16 around the chip and leads. Note further that Johnson uses both the words "pad" (col. 3, line 25) and "leads" (col. 3, line 32) in his disclosure, and, in so doing, distinguishes between those terms. To read Johnson's reference to "leads" as a reference to a mount pad overlooks this distinction. For at least these reasons, Appellant submits that Claim 1 is patentable over Johnson.

Claim 2 is also to a reel-to-reel tape. As noted above, Johnson does not disclose a reel-to-reel tape. Claim 2 includes the feature of "a chip mount pad in each of said second openings, attached to said first surface and shaped to be coplanar with said second surface." Johnson does not disclose such a chip mount pad. As mentioned above, element 10 in Johnson's Figure 6 is a lead, not a mount pad.

Claim 4 includes the feature "wherein said routing lines and contact lands are created by a photolithographic patterning and chemical etch process." Johnson does not disclose how his circuitry 2 is formed on dielectric 1. Note also that product-by-process Claim 4 depends from Claim 2, which is patentable over Johnson for the reasons presented above.

Claim 5 includes the feature "wherein said bending of said chip mount pad is provided by a mechanical coining process." Johnson does not disclose a coining process. Note also that product-by-process Claim 5 depends from Claim 2, which is patentable over Johnson for the reasons presented above.

Claim 6 includes the feature "wherein said first and second openings are created by a mechanical punching process." Johnson does not disclose a punching process. Note also that product-by-process Claim 6 depends from Claim 2, which is patentable over Johnson for the reasons presented above.

Claim 18 includes the feature of "a chip mount pad comprising a sheet of metal, a portion of said sheet of metal on said first surface of said substrate and a portion of said sheet of metal covering said opening such that said portion of said sheet of metal covering said opening is coplanar with said second surface of said substrate, said portion of said sheet of metal covering said opening having

first and second opposing surfaces, said second surface of said sheet of metal covering said opening being coplanar with said second surface of said substrate." Johnson does not teach or suggest a chip mount pad with the claimed features covering an opening. In Figure 6, even if Johnson's leads 10 are assumed for the sake of argument to be a chip mount pad, leads 10 clearly do not cover the opening in substrate 1. The Examiner has essentially admitted as much by stating that Johnson's leads 10 cover "at least part of said opening." Since Johnson is deficient in disclosing all of the claimed features, Appellant submits that Claim 18 is patentable over Johnson.

3. Claim 3 is patentable under 35 U.S.C. 103(a) over Johnson in view of Ikegami.

Claim 3 depends from Claim 2. As pointed out above, Johnson fails to disclose a chip mount pad as described in Claim 2. Johnson also fails to *suggest* such a pad. Ikegami, relied upon for its teaching of a particular arrangement of metals, does not cure this deficiency of Johnson. Therefore, Applicant submits that Claim 3 is patentable over the cited references.

4. Claims 8-11 are patentable under 35 U.S.C. 103(a) over Johnson in view of Cheng.

Claim 8 includes the feature of "a chip mount pad covering each of said second openings, attached to said first surface and shaped to be coplanar with said second surface." As indicated above, Johnson does not teach or suggest such a feature. Cheng, cited for its teaching of a particular bonding wire arrangement, does not cure this deficiency of Johnson. Since the combined references, taken individually or in combination, fail to disclose or suggest all of the claimed features, Appellant submits that Claim 8 is patentable over the cited combination of references. Claims 9-11 depend from Claim 8 and are therefore

patentable over Johnson in view of Cheng at least by virtue of their dependence from a patentable base claim.

5. Claims 19-24 are patentable under 35 U.S.C. 103(a) over Johnson in view of Carter.

Claims 19-21 depend from Claim 18, which, as indicated above, includes features not taught by Johnson. Specifically, Claim 18 includes the feature of "a chip mount pad comprising a sheet of metal, a portion of said sheet of metal on said first surface of said substrate and a portion of said sheet of metal covering said opening such that said portion of said sheet of metal covering said opening is coplanar with said second surface of said substrate, said portion of said sheet of metal covering said opening having first and second opposing surfaces, said second surface of said sheet of metal covering said opening being coplanar with said second surface of said substrate." As indicated above, Johnson does not disclose or suggest a mount pad covering an opening in a substrate. Carter does not cure that deficiency of Johnson. Carter's package is a leadframe-based package and thus does not include a substrate. A skilled artisan would therefore receive no motivation from Johnson or Carter to combine Carter's teachings with those of Johnson. Therefore, Appellant submits that Claims 19-21, which depend from Claim 18, are patentable over Johnson in view of Carter.

Claim 22 includes the feature of "a chip mount pad of metal foil attached to said first surface of said substrate and downset into and covering said opening such that a bottom surface of said chip mount pad is coplanar with said second surface of said substrate." Johnson does not disclose or suggest a chip mount pad downset into and covering an opening in a substrate. Carter does not cure that deficiency of Johnson. Carter's package is a leadframe-based package and thus does not include a substrate. The skilled artisan would therefore receive no motivation from Johnson or Carter to combine Carter's teachings with those of Johnson. Claims 23 and 24 depend from Claim 22. Appellant therefore submits

that Claims 23 and 24 are patentable over Johnson in view of Carter at least by virtue of their dependence from a patentable base claim.

6. Claims 25 and 26 are patentable under 35 U.S.C. 103(a) over Johnson in view of Cheng and Carter.

Claim 25 includes the feature of "a chip mount pad of metal foil attached to said first surface of said substrate and downset into and covering said opening such that a bottom surface of said chip mount pad is coplanar with said second surface of said substrate." Johnson does not disclose or suggest a chip mount pad downset into and covering an opening in a substrate. Neither Cheng nor Carter cures that deficiency of Johnson. Cheng does not disclose and opening or die mount pad as claimed. Carter's package is a leadframe-based package and thus does not include a substrate. The skilled artisan would therefore receive no motivation from Johnson or Carter or Cheng to combine Carter's teaching with those of Johnson and Cheng. Claim 26 depends from Claim 25 and is therefore patentable over Johnson in view of Carter and Cheng at least by virtue of its dependence upon a patentable base claim.

Claims 1-6 stand or fall together. Claims 8-11 and 18-21 stand or fall together. Claims 22-26 stand or fall together. Each of these groups of claims stand or fall independently of any other group of claims. The grouping of Claims 22-26 includes a downset feature that makes it separately patentable from the other groups of claims. The grouping of Claims 8-11 and 18-21 includes the feature of the chip mount pad covering an opening in the substrate. This feature makes this group separately patentable from the group of Claims 1-6. Therefore, Appellant requests that the claims be considered in these groupings.

Conclusion

In view of the above, Appellant appeals for the reversal of the rejections and allowance of Claims 1-6, 8-11, and 18-26.

Respectfully submitted,

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APPENDIX

Claims on Appeal

1. A reel-to-reel tape, having first and second surfaces, for use in the assembly of semiconductor chips, comprising:

a plurality of contact lands and a plurality of electrically conductive routing lines integral with said first surface of said tape; and

a chip mount pad, secured to said first surface, coplanar with said second surface.

2. A reel-to-reel tape, having first and second surfaces and first and second openings, for use in the assembly of semiconductor chips, comprising:

a plurality of electrically conductive routing lines and a plurality of contact lands on said first surface, covering said first openings in said tape; and

a chip mount pad in each of said second openings, attached to said first surface and shaped to be coplanar with said second surface.

3. The tape according to Claim 2 wherein said routing lines and contact lands are made of copper foil plated with nickel and gold.

4. The tape according to Claim 2 wherein said routing lines and contact lands are created by a photolithographic patterning and chemical etch process.

5. The tape according to Claim 2 wherein said bending of said chip mount pad is provided by a mechanical coining process.

6. The tape according to Claim 2 wherein said first and second openings are created by a mechanical punching process.

8. A low profile, high power semiconductor device including a plastic tape having first and second surfaces, comprising:

a plurality of electrically conductive routing lines and a plurality of contact lands on said first surface, said lands exposed by first openings in said tape;

second openings in said tape configured to accommodate integrated circuit chips;

a chip mount pad covering each of said second openings, attached to said first surface and shaped to be coplanar with said second surface;

a circuit chip mounted by means of a thermally conductive material on each of said chip mount pads;

bonding wires connecting said chip to said contact lands;

encapsulating material surrounding said first tape surface including each of said mounted chips and said wire bonds; and

solder balls attached to each of said exposed lands.

9. The semiconductor device according to Claim 8 wherein said chip mount pads, coplanar with said second tape surface, provide a direct thermal path to said circuit chips.

10. The semiconductor device according to Claim 8 wherein said chip mount pads serve as heat convection surface for said circuit chips.

11. The semiconductor device according to Claim 8 wherein said device is created by a transfer molding process of molding compounds, thereby providing mechanical rigidity to said device even when the device thickness is kept to a low profile.

18. A packaged integrated circuit, comprising:

a substrate having first and second opposing surfaces; said substrate including an opening extending through said substrate from said first surface to said second surface;

a chip mount pad comprising a sheet of metal, a portion of said sheet of metal on said first surface of said substrate and a portion of said sheet of metal covering said opening such that said portion of said sheet of metal covering said opening is coplanar with said second surface of said substrate, said portion of said sheet of metal covering said opening having first and second opposing surfaces, said second surface of said sheet of metal covering said opening being coplanar with said second surface of said substrate;

an integrated circuit chip mounted on said first surface of said sheet of metal in said opening.

19. The packaged integrated circuit of Claim 18, further comprising encapsulant covering at least a portion of said first surface of said substrate and said chip, wherein said encapsulant does not cover said second surface of said substrate and does not cover said portion of said sheet of metal covering said opening that is coplanar with said second surface of said substrate.

20. The packaged integrated circuit of Claim 18, further comprising a heatsink attached to said second surface of said sheet of metal covering said opening.

21. The packaged integrated circuit of Claim 18, wherein said second surface of said sheet of metal covering said opening is attached to a printed circuit board.

22. A packaged integrated circuit chip, comprising:

a substrate having first and second opposing surfaces; said substrate including an opening extending through said substrate from said first surface to said second surface;

a chip mount pad of metal foil attached to said first surface of said substrate and downset into and covering said opening such that a bottom surface of said chip mount pad is coplanar with said second surface of said substrate;

an integrated circuit chip mounted on a top surface of said chip mount pad;

encapsulation on said first surface of said substrate and not on said second surface of said substrate, such that said encapsulation covers said chip, but does not cover said bottom surface of said chip mount pad.

23. The packaged integrated circuit of Claim 22, further comprising a heatsink attached to said bottom surface of said chip mount pad.

24. The packaged integrated circuit of Claim 22, wherein said bottom surface of said chip mount pad is attached to a printed circuit board.

25. A packaged integrated circuit chip, comprising:

a substrate having first and second opposing surfaces; said substrate including an opening extending through said substrate from said first surface to said second surface, said opening having a first size;

a plurality of contact lands on said first surface of said substrate adjacent to said opening;

a chip mount pad of metal foil attached to said first surface of said substrate and downset into and covering said opening such that a bottom surface of said chip mount pad is coplanar with said second surface of said substrate;

an integrated circuit chip mounted on a top surface of said chip mount pad, said integrated circuit chip having a second size, wherein said second size is smaller than said first size;

bond wires coupling said integrated circuit chip to said contact lands; and

encapsulation on said first surface of said substrate and not on said second surface of said substrate, such that said encapsulation covers said chip, bond wires, and contact lands, but does not cover said bottom surface of said chip mount pad.

26. The packaged integrated circuit of Claim 25, wherein said substrate is plastic tape.